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MEMC 98-3052/2512.2 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Robert J. Falster. Serial No. 10/038,084 —— Filed January 3, 2002 Confirmation No. 7363

For SILICON ON INSULATOR STRUCTURE HAVING A LOW DEFECT DENSITY DEVICE LAYER AND A PROCESS FOR THE PREPARATION THEREOF

May 14, 2002

TO THE COMMISSIONER OF PATENTS AND TRADEMARKS,

SIR:

INFORMATION DISCLOSURE STATEMENT

In accordance with 37 C.F.R. 1.97 and 1.98 and MPEP 609, and in compliance with the duty of disclosure set forth in 37 C.F.R. 1.56, applicants submit copies of the references listed on the attached PTO/SB/08A for consideration by the Patent and Trademark Office in the above-entitled application and to be made of record therein.

This application is a divisional of U.S. Application Serial No. 09/737,715, filed December 15, 2000. Pursuant to M.P.E.P. §609, Applicants are not submitting copies of Reference Nos. 1-23, 25-33, 35-55, 58-59, 61, 63-72, 74-109, 111-118 and 121-132, which were previously made of record in application Serial No. 09,737,715. Applicants are enclosing herewith copies of Reference Nos. 24, 34, 56-57, 60, 62, 73, 110 and 119-120.

Please note that there were several translations previously submitted with Application Serial No. 09/737,715, as well as new translations submitted herewith, and Applicants make no representation as to accuracy or completeness of those translations.

The Commissioner is hereby authorized to charge any fees incurred regarding this Information Disclosure Statement to Account No. 19-1345 if an Office Action was issued prior to the date of mailing of this Statement.

MEMC 98-3052/2512.2 **PATENT**

Respectfully submitted,

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RAS/TFM/dmt *Enclosures

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